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10/820,643	04/08/2004	Matthew Bellantoni	CDS-007	8477

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GOODWIN PROCTER LLP
PATENT ADMINISTRATOR
EXCHANGE PLACE
BOSTON, MA 02109-2881

EXAMINER	
GUILL, RUSSELL L	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,643	BELLANTONI ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/31/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 - 53 have been examined. Claims 1 - 53 have been rejected.

Information Disclosure Statement

2. The information disclosure statement filed January 31, 2005 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because references C2, C4, C9, C40, C43, C44, C46 and C47 do not include a date. It has been placed in the application file, but the information referred to in the recited references have not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. **Claims 1 - 53** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. Regarding independent claim 1 and dependent claims, in order to be statutory, the claim must either perform a physical transformation, or have a practical application having a useful, concrete and tangible result. The claim does not appear to perform a physical transformation, nor have a useful and

tangible result, and is therefore non-statutory. The claim appears to only perform data manipulation, and can be interpreted as an entirely abstract process.

b. Regarding independent claim 32 and dependent claims, the recited apparatus appears to perform abstract operations such as setting a destination variable equal to a source variable, and therefore, in order to be statutory, the claim must either perform a physical transformation, or have a practical application having a useful, concrete and tangible result. The claim does not appear to perform a physical transformation, nor have a useful and tangible result, and is therefore non-statutory. The claim appears to only perform data manipulation, and does not appear to have a tangible result.

c. Regarding independent claim 32 and dependent claims, the claim is directed to an apparatus that appears to be entirely software (i.e., a software apparatus), and is therefore at best, a collection of functional descriptive material. Further, the claim allows an interpretation that is source code, which is non-functional descriptive material. Neither a collection of functional descriptive material nor non-functional descriptive material is statutory.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. **Claims 1, 3 - 14, 16 - 23, 25 - 31, 32, 34 - 40 and 42 - 53** are rejected under 35 U.S.C. 103(a) as being unpatentable over Jex (U.S. Patent Number 5,598,113) in view of Wang (U.S. Patent Number 6,134,516).

a. The art of Jex is directed to an asynchronous parallel synchronizer that can be used to interconnect two processor systems within a multiple processor system (*Abstract*).

b. The art of Wang is directed to a simulation and emulation system implemented in hardware and software (*column 1, lines 10 - 20*).

c. The art of Jex and the art of Wang are analogous art because they both contain the art of interfaces between asynchronous systems (*Jex, column 1, lines 5 - 13; Wang, figure 10*).

d. Regarding **claim 1**:

e. Jex appears to teach:

f. providing a plurality of hardware objects, each representing at least a portion of a design of a hardware device (*figure 9, elements 850, 860*);

g. providing an interconnection object (*figure 9, element 960a*) in communication with (i) at least a first hardware object (*figure 9, element 860*) and (ii) at least a second hardware object (*figure 9, element 850*), ~~the interconnection object including a source variable and a destination variable~~;

h. storing, by the at least one interconnection object, output data from the at least one first hardware object in the source variable, the output data being intended for receipt by the at least one second hardware object (*figure 9, elements 860, 971a, 960a, 850; it would have been obvious that output data from the first hardware object was stored in a source variable in the interconnection object*);

i. setting the destination variable equal to the source variable based at least in part on receipt of an update command (*figure 9, element 920*).; and

j. causing the at least one second hardware object to receive data from the destination variable as input (*figure 9, elements 960a, 973a, 850*).

k. Jex does not specifically teach (in ***bold italic underline***):

l. providing an interconnection object in communication with (i) at least a first hardware object and (ii) at least a second hardware object, ***the interconnection object including a source variable and a destination variable***;

m. Wang appears to teach:

n. providing an interconnection object in communication with (i) at least a first hardware object and (ii) at least a second hardware object, ***the interconnection object including a source variable and a destination variable*** (*figure 19, elements 516 and 517*);

o. The motivation to use the art of Wang with the art of Jex would have been the benefit recited in Wang that double buffering avoids disturbing internal

hardware states which may cause race conditions (*column 39, lines 46 - 51*), which would have been recognized as a benefit by the ordinary artisan.

p. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Wang with the art of Jex to produce the claimed invention.

q. Regarding **claim 32**:

r. Jex appears to teach

s. at least one first hardware object and at least one second hardware object, each hardware object representing at least a portion of a design of a hardware device (*figure 9, elements 850, 860*);

t. at least one interconnection object (*figure 9, element 960a*) in communication with the at least one first hardware object (*figure 9, element 860*) and the at least one second hardware object (*figure 9, element 850*), wherein the at least one interconnection object ~~includes a source variable and a destination variable and~~ is responsive to an update command (*figure 9, element 920*), the interconnection object being configured to (i) receive, in the source variable, output data from the at least one first hardware object intended for receipt by the at least one second hardware object (*figure 9, elements 860, 971a, 960a, 850; it would have been obvious that output data from the first hardware object was stored in a source variable in the interconnection object*), (ii) set the destination variable equal to the source variable based at least in part on receipt of the update command (*figure 9, element 920*), and (iii) thereupon provide to the at least one second hardware object data from the destination variable as input (*figure 9, elements 960a, 973a, 850*).

u. Jex does not specifically teach (in ***bold italic underline***):

v. at least one interconnection object in communication with the at least one first hardware object and the at least one second hardware

object, wherein the at least one interconnection object ***includes a source variable and a destination variable*** and is responsive to an update command, the interconnection object being configured to (i) receive, in the source variable, output data from the at least one first hardware object intended for receipt by the at least one second hardware object, (ii) set the destination variable equal to the source variable based at least in part on receipt of the update command, and (iii) thereupon provide to the at least one second hardware object data from the destination variable as input.

w. Wang appears to teach:

x. at least one interconnection object in communication with the at least one first hardware object and the at least one second hardware object, wherein the at least one interconnection object ***includes a source variable and a destination variable*** (*figure 19, elements 516 and 517*);

y. The motivation to use the art of Wang with the art of Jex would have been the benefit recited in Wang that double buffering avoids disturbing internal hardware states which may cause race conditions (*column 39, lines 46 - 51*), which would have been recognized as a benefit by the ordinary artisan.

z. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Wang with the art of Jex to produce the claimed invention.

aa. Regarding **claims 3 and 34**:

bb. Jex appears to teach:

cc. the output data is based at least in part on a plurality of values supplied by the at least one first hardware object (*figure 9, element 971a; column 9, lines 60 - 65; it would have been obvious that bus 971a had multiple bits which were a plurality of values*).

dd. Regarding **claims 4 and 35**:

ee. Jex does not specifically teach:

ff. the output data is based at least in part on a random function.

gg. Wang appears to teach:

hh. the output data is based at least in part on a random function (*figures 29 and 30, column 117, lines 21 - 50; S9 generates a random sigin*).

ii. Regarding **claims 5 and 36**:

jj. Jex does not specifically teach:

kk. the output data is based at least in part on a resolution function.

ll. Wang appears to teach:

mm. the output data is based at least in part on a resolution function (*column 34, lines 13 - 31; it would have been obvious that a multiplexer was a resolution function*).

nn. Regarding **claim 6**:

oo. Jex does not specifically teach:

pp. the source variable comprises output data from a plurality of hardware objects.

qq. Wang appears to teach:

rr. the source variable comprises output data from a plurality of hardware objects (*figure 35c, element 1097, the bits on the bus 1097 come from different hardware objects 1092 and 1093*).

ss. Regarding **claim 7**:

tt. Jex does not specifically teach:

uu. the update command is received after a signal transition.

vv. Wang appears to teach:

ww. the update command is received after a signal transition (*column 39, lines 60 - 63*).

xx. Regarding **claim 8**:

yy. Jex does not specifically teach:

zz. the signal transition comprises a clock pulse.

aaa. Wang appears to teach:

bbb. the signal transition comprises a clock pulse (*column 39, lines 60 - 63*).

ccc. Regarding **claim 9**:

ddd. Jex does not specifically teach:

eee. the signal transition comprises a reset.

fff. Wang appears to teach:

ggg. the signal transition comprises a reset (*figure 18b, design flip-flop, signal R is reset*).

hhh. Regarding **claim 10**:

iii. Jex does not specifically teach:

jjj. the signal transition is based at least in part on an arbitrary function.

kkk. Wang appears to teach:

lll. the signal transition is based at least in part on an arbitrary function (*column 39, lines 60 - 63; a clock is an arbitrary function*).

mmm. Regarding **claims 11 and 37**:

nnn. Jex does not specifically teach:

ooo. the at least one first hardware object and the at least one second hardware object reside within separate computational processes.

ppp. Wang appears to teach:

qqq. the at least one first hardware object and the at least one second hardware object reside within separate computational processes (*figure 45, elements 1101, 1102, 1103, 1104; it would have been obvious that a simulation workstation with multiple cpu's would process hardware objects in separate computational processes*).

rrr. Regarding **claims 12 and 38**:

sss. Jex does not specifically teach:

ttt. the at least one first hardware object and the at least one second hardware object are executed by different processors.

uuu. Wang appears to teach:

vvv. the at least one first hardware object and the at least one second hardware object are executed by different processors (*figure 45, elements 1101, 1102, 1103, 1104*).

www. Regarding **claims 13 and 39**:

xxx. Jex does not specifically teach:

yyy. the at least one first hardware object and the at least one second hardware object reside on different computers.

zzz. Wang appears to teach:

aaaa. the at least one first hardware object and the at least one second hardware object reside on different computers (*figure 45, elements 1101, 1102, 1103, 1104; it would have been obvious that different cpu's were different computers*).

bbbb. Regarding **claim 14 and 40**:

cccc. Jex does not specifically teach:

dddd. the source variable contains a plurality of source data values.

eeee. Wang appears to teach:

ffff. the source variable contains a plurality of source data values (*figure 35c, element 1097, the bits on the bus 1097 come from different*

hardware objects 1092 and 1093, which are a plurality of source data values).

gggg. Regarding **claims 16 and 42**:

hhhh. Jex appears to teach:

iiii. the plurality of source data values comprises a plurality of states of at least one pin of a hardware device corresponding to the at least one first hardware object (*figure 9, element 971a; it would have been obvious that there was at least one pin of the hardware device 860, and the states of the pin would have been at least a plurality of states since a binary state is a plurality of states*).

jjjj. Regarding **claim 17**:

kkkk. Jex does not specifically teach:

llll. the plurality of source data values comprises at least one state of a plurality of pins of at least one hardware device corresponding to the at least one first hardware object.

mmmm. Wang appears to teach:

nnnn. the plurality of source data values comprises at least one state of a plurality of pins of at least one hardware device corresponding to the at least one first hardware object (*figure 35d, element 1097; it would have been obvious that hardware device 1095 had a plurality of pins producing a state value*).

oooo. Regarding **claims 18 and 43**:

pppp. Jex does not specifically teach:

qqqq. the at least one first hardware object corresponds to at least one bus, the plurality of source data values comprising a plurality of states of the at least one bus.

rrrr. Wang appears to teach:

ssss. the at least one first hardware object corresponds to at least one bus, the plurality of source data values comprising a plurality of states of the at least one bus (*figure 1, element 50, PCI bus*).

tttt. Regarding **claims 19**:

uuuu. Jex does not specifically teach:

vvvv. the plurality of source data values comprises at least one state of a plurality of buses.

wwww. Wang appears to teach:

xxxx. the plurality of source data values comprises at least one state of a plurality of buses (*figure 1, elements 50 and 52, PCI bus 0 and PCI bus 1*).

yyyy. Regarding **claims 20**:

zzzz. Jex does not specifically teach:

aaaaa. the step of providing a resolution function to accommodate multiple drivers for a single bus or signal.

bbbbb. Wang appears to teach:

ccccc. the step of providing a resolution function to accommodate multiple drivers for a single bus or signal (*column 34, lines 13 - 31; it would have been obvious that a multiplexer was a resolution function that could accommodate multiple drivers for a single bus or signal*).

ddddd. Regarding **claims 44**:

eeeee. Jex does not specifically teach:

fffff. the interconnection object comprises means for executing a resolution function to accommodate different bus types.

ggggg. Wang appears to teach:

hhhhh. the interconnection object comprises means for executing a resolution function to accommodate different bus types (*column 34,*

lines 13 - 31; it would have been obvious that a multiplexer was a resolution function that could accommodate different bus types).

iiiii. Regarding **claims 21 and 45**:

jjjjj. Jex does not specifically teach:

kkkkk. the plurality of source data values comprises a plurality of states of at least one control signal coming from the at least one first hardware object.

lllll. Wang appears to teach:

mmmmm. the plurality of source data values comprises a plurality of states of at least one control signal coming from the at least one first hardware object (*figure 53, element 1232; it would have been obvious that command was a control signal*).

nnnnn. Regarding **claims 22 and 46**:

ooooo. Jex does not specifically teach:

ppppp. the plurality of source data values comprises at least one state of a plurality of control signals coming from the at least one first hardware object

qqqqq. Wang appears to teach:

rrrrr. the plurality of source data values comprises at least one state of a plurality of control signals coming from the at least one first hardware object (*figure 53, element 1232; it would have been obvious that command was a control signal*).

sssss. Regarding **claim 23 and 47**:

ttttt. Jex does not specifically teach:

uuuuu. the destination variable contains a plurality of destination data values.

vvvvv. Wang appears to teach:

wwwww. the destination variable contains a plurality of destination data values (*figure 35c, element 1097, the bits on the bus 1097 come from different hardware objects 1092 and 1093, which supply a plurality of destination data values*).

xxxxx. Regarding **claim 25 and 48**:

yyyyy. Jex appears to teach:

zzzzz. the plurality of destination data values comprises a plurality of states of at least one pin of the at least one second hardware object (*figure 9, element 973a; it would have been obvious that there was at least one pin of the hardware device 850, and the states of the pin would have been at least a plurality of states since binary states are a plurality of states*).

aaaaaa. Regarding **claim 26**:

bbbbbb. Jex does not specifically teach:

cccccc. the plurality of destination data values comprises at least one state of a plurality of pins of the at least one second hardware object.

dddddd. Wang appears to teach:

eeeeee. the plurality of destination data values comprises at least one state of a plurality of pins of the at least one second hardware object (*figure 35d, element 1097; it would have been obvious that hardware device 1094 had a plurality of pins producing a state value*).

ffffff. Regarding **claims 27 and 49**:

gggggg. Jex does not specifically teach:

hhhhhh. the plurality of destination data values comprises a plurality of states of at least one bus.

iiiiii. Wang appears to teach:

jjjjjj. the plurality of destination data values comprises a plurality of states of at least one bus (*figure 1, element 50, PCI bus*).

kkkkkk. Regarding **claims 28 and 50**:

llllll. Jex does not specifically teach:

mmmmmm. the plurality of destination data values comprises at least one state of each of a plurality of buses.

nnnnnn. Wang appears to teach:

oooooo. the plurality of destination data values comprises at least one state of each of a plurality of buses (*figure 1, elements 50 and 52, PCI bus 0 and PCI bus 1*).

pppppp. Regarding **claims 29**:

qqqqqq. Jex does not specifically teach:

rrrrrr. the step of providing a resolution function to accommodate different bus types.

ssssss. Wang appears to teach:

tttttt. the step of providing a resolution function to accommodate different bus types (*column 34, lines 13 - 31; it would have been obvious that a multiplexer was a resolution function that could accommodate different bus types*).

uuuuuu. Regarding **claims 51**:

vvvvvv. Jex does not specifically teach:

wwwwww. the interconnection object comprises means for executing a resolution function to accommodate multiple drivers for a single bus or signal.

xxxxxx. Wang appears to teach:

yyyyyy. the interconnection object comprises means for executing a resolution function to accommodate multiple drivers for a single bus or signal (*column 34, lines 13 - 31; it would have been obvious that a*

multiplexer was a resolution function that could accommodate multiple drivers for a single bus or signal).

zzzzzz. Regarding **claims 30 and 52**:

aaaaaaa. Jex does not specifically teach:

bbbbbbb. the plurality of destination data values comprises a plurality of states of at least one control signal going to the at least one second hardware object.

ccccccc. Wang appears to teach:

ddddddd. the plurality of destination data values comprises a plurality of states of at least one control signal going to the at least one second hardware object (*figure 53, element 1232; it would have been obvious that command was a control signal*).

eeeeeee. Regarding **claims 31 and 53**:

fffffff. Jex does not specifically teach:

ggggggg. the plurality of destination data values comprises at least one state of a plurality of control signals going to the at least one second hardware object.

hhhhhhh. Wang appears to teach:

iiiiiii. the plurality of destination data values comprises at least one state of a plurality of control signals going to the at least one second hardware object (*figure 53, element 1232; it would have been obvious that command was a control signal*).

8. **Claims 2 and 33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Jex as modified by Wang as applied to claims 1, 3 - 14, 16 - 23, 25 - 31, 32, 34 - 40 and 42 - 53 above, further in view of Mano (M. Morris Mano; "Computer System Architecture", second edition, 1982, Prentice-Hall, pages 59 - 62, 277 - 278, 426 - 428).

a. Jex as modified by Wang teaches a method and apparatus for simulating hardware parallelism as recited in claims 1, 3 - 14, 16 - 23, 25 - 31, 32, 34 - 40 and 42 - 53 above.

b. The art of Mano is directed to the design of computer systems (*Title*).

c. The art of Mano and the art of Jex as modified by Wang are analogous art because they are both directed to the art of designing digital devices, including FIFO devices (*Jex, figure 9; Mano, page 426*).

d. The motivation to use the art of Mano with the art of Jex would have been the benefit recited in Mano that a FIFO device is useful in some applications when data is transferred asynchronously (*page 426, section "First-In First-Out (FIFO) Buffer*), which would have been recognized as a benefit by the ordinary artisan.

e. Regarding **claims 2 and 33**:

f. Jex does not specifically teach:

g. the at least one first hardware object and the at least one second hardware object are the same hardware object.

h. Mano appears to teach:

i. the at least one first hardware object and the at least one second hardware object are the same hardware object (*page 277, last paragraph, and page 278, first paragraph; a pipeline is inside a processor, so the pipeline is connected to the same hardware object*).

j. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mano with the art of Jex as modified by Wang to produce the claimed invention.

9. **Claims 15, 24 and 41** are rejected under 35 U.S.C. 103(a) as being unpatentable over Jex as modified by Wang as applied to claims 1, 3 - 14, 16 - 23, 25 - 31, 32, 34 - 40 and 42 - 53 above, further in view of Patterson (David A. Patterson et al.; "Computer

Architecture A Quantitative Approach", 1996, Morgan Kaufmann Publishers, pages 179 and 504).

a. Jex as modified by Wang teaches a method and apparatus for simulating hardware parallelism as recited in claims 1, 3 - 14, 16 - 23, 25 - 31, 32, 34 - 40 and 42 - 53 above.

b. The art of Patterson is directed to the design of computer systems (*Title*).

c. The art of Patterson and the art of Jex as modified by Wang are analogous art because they are both directed to the art of designing digital devices.

d. The motivation to use the art of Patterson with the art of Jex would have been the knowledge of the ordinary artisan that exception handling was necessary in a pipelined computer (*page 179, section "Dealing with Exceptions"*).

e. Regarding **claims 15 and 41**:

f. Jex does not specifically teach:

g. the step of detecting illegal source data values and preventing their storage in the source variable.

h. Patterson appears to teach:

i. the step of detecting illegal source data values and preventing their storage in the source variable (*page 179, section "Dealing with Exceptions"*).

j. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Patterson with the art of Jex as modified by Wang to produce the claimed invention.

k. Regarding **claim 24**:

l. Jex does not specifically teach:

m. the step of detecting illegal destination data values and preventing their storage in the destination variable.

n. Patterson appears to teach:

o. the step of detecting illegal destination data values and preventing their storage in the destination variable (*page 179, section "Dealing with Exceptions"*).

10. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the Applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. The entire reference is considered to provide disclosure relating to the claimed invention.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure:

a. Klein (U.S. Patent Application Publication 2004/0064430) teaches updating data in a queue (paragraphs [0028] - [0030].

b. Hori (U.S. Patent Number 5,943,509) teaches a FIFO queue between a pair of processors.

c. Powell (U.S. Patent Application Publication 2002/0183997) teaches an interface with a source and destination variable.

d. Tiberiu Chelcea et al.; "Robust Interfaces for Mixed-Timing Systems with Application to Latency-Insensitive Protocols", 2001, Design Automation Conference, six unnumbered pages; teaches a FIFO for interfacing between hardware modules.

e. Anoop Iyer et al.; "Power and Performance Evaluation of Globally Asynchronous Locally Synchronous Processors", 2002, Proceedings of the 29th Annual International Symposium on Computer Architecture, pages 1 - 11; teaches a FIFO for interfacing between hardware modules, see page 4.

f. Jie Liu et al.; "Software Timing Analysis Using HW/SW Cosimulation and Instruction Set Simulator", 1998, Proceedings of the Sixth International Workshop on Hardware/Software Codesign, pages 65 - 69; teaches a FIFO for interfacing between hardware modules, see page 65, right-side column, "Stars talk to each other . . .".

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100